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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,251	11/27/2001	Franck Roche	00RO30354280	1363

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EXAMINER	
YANCHUS III, PAUL B	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,251	ROCHE ET AL.	
	Examiner	Art Unit	
	Paul B. Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *15-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *45-53* is/are allowed.

6)☒ Claim(s) *15-19, 22, 24-29, 32, 34-39, 41, 43, 44, 54-56, 59, 61 and 62* is/are rejected.

7)☒ Claim(s) *20,21,23,30,31,33,40,42,57,58 and 60* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This non-final office action is in response to communications filed on 4/4/05.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15-19, 22, 24-29, 32, 34-39, 41, 43, 44, 54-56, 59, 61 and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA], in view of, Farnworth et al., US Patent no. 6,605,956[1] [Farnworth].

Regarding claim 15, AAPA discloses a microprocessor comprising:

a first terminal receiving a mode selection signal [P1 in Figure 1];

a second terminal for receiving a control signal [RESET in Figure 1]; and

a selection means [CNTR and DEC in Figure 1] connected to the first and second terminals for selecting an operating mode of the microprocessor based upon the mode selection signal and the control signal, said selection means comprising a counter [CNTR in Figure 1] having a counting input [E1 in Figure 1] and a reset input [E2 in Figure 1], first coupling means coupling the counting input the first terminal, second coupling means coupling the reset input to the second terminal [page 1, lines 7-23].

AAPA does not disclose a default means for maintaining by default the reset input at a first logic value for ensuring that said counter is maintained at zero in an absence of the control signal. Farnworth discloses a default means [Switching Circuit, Impedance Circuit and Voltage Circuit in Figure 6A] for ensuring that an IC device does not accidentally enter a test mode of operation by holding a test mode determining signal at a constant value [column 5, line 49 – column 6, line 10]. It would have been obvious to one of ordinary skill in the art to insert the Farnworth default means into the AAPA system in order to selectively disable a test mode to ensure that the test mode is not accidentally entered by a user [column 2, lines 16-23].

Regarding claims 16 and 17, Farnworth states that the default means may be located internally or externally to the IC [column 4, lines 59-63].

Regarding claim 18, Farnworth states that the impedance element may be a resistor [column 5, lines 63-65].

Regarding claim 19, Farnworth discloses placing the default means between a test mode initiation input [bond pad] and the counter [function circuit]. Farnworth further discloses programming the default means to enable or disable the connection between the test mode initiation input and the counter [column 6, lines 1-20].

Regarding claim 22, AAPA further discloses:

a decoder [DEC in Figure 1] connected to an output of said counter for delivering at least one mode bit, with a value of each mode bit being based upon a counting result delivered by said counter [Figure 1 and page 2, lines 10-17]; and

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[1] included in previous office action mailed on 12/3/04.

a central processing unit [CPU in Figure 1] connected to an output of said decoder for receiving the at least one mode bit [page2, lines 16-24].

Regarding claim 24, AAPA states that the operating mode is a test mode or a servicing mode requiring application of a predetermined number of pulses to the counting input of said counter during a selection period for selecting the operating mode of the microprocessor [page 2, lines 6-9 and page 3, lines 3-12].

Regarding claim 25, AAPA and Farnsworth do not specifically state that the first and second terminals are used as I/O ports of the microprocessor when the microprocessor is operating outside of a mode selection period. However, it would have been obvious to one of ordinary skill in the art to use the first and second terminals for a second function when they are not needed for a first function. Using pins on a microprocessor to perform different functions at different microprocessor operating periods reduces the number of pins needed by the microprocessor and therefore reduces the size and complexity of the microprocessor.

Regarding claim 26, AAPA discloses a microprocessor comprising:

a first terminal receiving a mode selection signal [P1 in Figure 1];

a second terminal for receiving a control signal [RESET in Figure 1]; and

a selection circuit [CNTR and DEC in Figure 1] connected to the first and second terminals for selecting an operating mode of the microprocessor based upon the mode selection signal and the control signal, said selection circuit comprising a counter [CNTR in Figure 1] having a counting input [E1 in Figure 1] and a reset input [E2 in Figure 1], first coupling circuit coupling the counting input the first terminal, second coupling circuit coupling the reset input to the second terminal [page 1, lines 7-23].

AAPA does not disclose a device for maintaining by default the reset input at a first logic value for ensuring that said counter is maintained at zero in an absence of the control signal. Farnworth discloses a device [Switching Circuit, Impedance Circuit and Voltage Circuit in Figure 6A] for ensuring that an IC device does not accidentally enter a test mode of operation by holding a test mode determining signal at a constant value [column 5, line 49 – column 6, line 10]. It would have been obvious to one of ordinary skill in the art to insert the Farnworth default means into the AAPA system in order to selectively disable a test mode to ensure that the test mode is not accidentally entered by a user [column 2, lines 16-23].

Regarding claims 27 and 28, Farnworth states that the device may include a resistor [column 5, lines 63-65]. Farnworth also states that the device may be located internally or externally to the IC [column 4, lines 59-63].

Regarding claim 29, Farnworth discloses placing the device between a test mode initiation input [bond pad] and the counter [function circuit]. Farnworth further discloses programming the device to enable or disable the connection between the test mode initiation input and the counter [column 6, lines 1-20].

Regarding claim 32, AAPA further discloses:

a decoder [DEC in Figure 1] connected to an output of said counter for delivering at least one mode bit, with a value of each mode bit being based upon a counting result delivered by said counter [Figure 1 and page 2, lines 10-17]; and

a central processing unit [CPU in Figure 1] connected to an output of said decoder for receiving the at least one mode bit [page 2, lines 16-24].

Regarding claim 34, AAPA states that the operating mode is a test mode or a servicing mode requiring application of a predetermined number of pulses to the counting input of said counter during a selection period for selecting the operating mode of the microprocessor [page 2, lines 6-9 and page 3, lines 3-12].

Regarding claim 35, AAPA and Farnsworth do not specifically state that the first and second terminals are used as I/O ports of the microprocessor when the microprocessor is operating outside of a mode selection period. However, it would have been obvious to one of ordinary skill in the art to use the first and second terminals for a second function when they are not needed for a first function. Using pins on a microprocessor to perform different functions at different microprocessor operating periods reduces the number of pins needed by the microprocessor and therefore reduces the size and complexity of the microprocessor.

Regarding claim 36, AAPA discloses a method for selecting an operating mode of a microprocessor comprising a counter [CNTR in Figure 1] having a counting input [E1 in Figure 1] and a reset input [E2 in Figure 1], and a first coupling circuit coupling the counting input to a first terminal of the microprocessor, and a second coupling circuit coupling the reset input to a second terminal of the microprocessor [page 1, lines 7-23], the method comprising:

driving the counting input with a mode selection signal applied to the first terminal of the microprocessor [P1 in Figure 1 and page 1, lines 7-23]; and

driving the reset input by a control signal applied to the second terminal [RESET in Figure 1 and page 1, lines 7-23] for activating the counter.

AAPA does not disclose maintaining by default the reset input at a first logic value for ensuring that the counter is maintained at a predetermined value in an absence of the control

signal. Farnworth discloses a device [Switching Circuit, Impedance Circuit and Voltage Circuit in Figure 6A] for ensuring that an IC device does not accidentally enter a test mode of operation by holding a test mode determining signal at a constant value [column 5, line 49 – column 6, line 10]. It would have been obvious to one of ordinary skill in the art to insert the Farnworth device into the AAPA system in order to selectively disable a test mode to ensure that the test mode is not accidentally entered by a user [column 2, lines 16-23].

Regarding claims 37 and 38, Farnworth states that the device may include a resistor [column 5, lines 63-65]. Farnworth also states that the default maintaining means may be located internally or externally to the IC [column 4, lines 59-63].

Regarding claim 39, Farnworth discloses placing the default maintaining means between a test mode initiation input [bond pad] and the counter [function circuit]. Farnworth further discloses programming the default maintaining means to enable or disable the connection between the test mode initiation input and the counter [column 6, lines 1-20].

Regarding claim 41, AAPA further discloses that the selection signal includes a predetermined number of pulses and using the counter for counting the number of pulses in the mode selection signal [page 2, lines 6-9 and page 3, lines 3-12], generating at least one mode bit based upon the number of pulses counted, and delivering the at least one mode bit to a central processing unit [Figure 1 and page 2, lines 10-24].

Regarding claim 43, AAPA states that the operating mode is a test mode or a servicing mode requiring application of a predetermined number of pulses to the counting input of said counter during a selection period for selecting the operating mode of the microprocessor [page 2, lines 6-9 and page 3, lines 3-12].

Regarding claim 44, AAPA and Farnsworth do not specifically state that the first and second terminals are used as I/O ports of the microprocessor when the microprocessor is operating outside of a mode selection period. However, it would have been obvious to one of ordinary skill in the art to use the first and second terminals for a second function when they are not needed for a first function. Using pins on a microprocessor to perform different functions at different microprocessor operating periods reduces the number of pins needed by the microprocessor and therefore reduces the size and complexity of the microprocessor.

Regarding claim 54, AAPA discloses a microprocessor comprising:

a first terminal receiving a mode selection signal [P1 in Figure 1];

a second terminal for receiving a control signal [RESET in Figure 1]; and

a selection circuit [CNTR and DEC in Figure 1] connected to the first and second terminals for selecting an operating mode of the microprocessor based upon the mode selection signal and the control signal, said selection circuit comprising a counter [CNTR in Figure 1] having a counting input [E1 in Figure 1] and a reset input [E2 in Figure 1], first coupling circuit coupling the counting input the first terminal, second coupling circuit coupling the reset input to the second terminal [page 1, lines 7-23].

AAPA does not disclose a device for maintaining by default the reset input at a first logic value for ensuring that said counter is maintained at zero in an absence of the control signal. Farnworth discloses a device [Switching Circuit, Impedance Circuit and Voltage Circuit in Figure 6A] for ensuring that an IC device does not accidentally enter a test mode of operation by holding a test mode determining signal at a constant value [column 5, line 49 – column 6, line 10]. Farnworth discloses placing the device between a test mode initiation input [bond pad] and

the counter [function circuit]. Farnworth further discloses programming the device to enable or disable the connection between the test mode initiation input and the counter [column 6, lines 1-20]. It would have been obvious to one of ordinary skill in the art to insert the Farnworth default means into the AAPA system in order to selectively disable a test mode to ensure that the test mode is not accidentally entered by a user [column 2, lines 16-23].

Regarding claims 55 and 56, Farnworth states that the device may include a resistor [column 5, lines 63-65]. Farnworth also states that the device may be located internally or externally to the IC [column 4, lines 59-63].

Regarding claim 59, AAPA further discloses:

a decoder [DEC in Figure 1] connected to an output of said counter for delivering at least one mode bit, with a value of each mode bit being based upon a counting result delivered by said counter [Figure 1 and page 2, lines 10-17]; and

a central processing unit [CPU in Figure 1] connected to an output of said decoder for receiving the at least one mode bit [page 2, lines 16-24].

Regarding claim 61, AAPA states that the operating mode is a test mode or a servicing mode requiring application of a predetermined number of pulses to the counting input of said counter during a selection period for selecting the operating mode of the microprocessor [page 2, lines 6-9 and page 3, lines 3-12].

Regarding claim 62, AAPA and Farnsworth do not specifically state that the first and second terminals are used as I/O ports of the microprocessor when the microprocessor is operating outside of a mode selection period. However, it would have been obvious to one of ordinary skill in the art to use the first and second terminals for a second function when they are

not needed for a first function. Using pins on a microprocessor to perform different functions at different microprocessor operating periods reduces the number of pins needed by the microprocessor and therefore reduces the size and complexity of the microprocessor.

Allowable Subject Matter

Claims 45-53 are allowed.

Claims 20, 21, 23, 30, 31, 33, 40, 42, 57, 58 and 60 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Paul Yanchus
June 9, 2005